For Technology
in Quality

User's Manual

TQM8315M

TQM8315M UM 106

29.10.2010

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1. About this manual

This manual contains technical information concerning the Minimodule TQM8315M.

1.1 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.2 Terms and conventions

Symbol / Tag	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed with the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages greater than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Filename.ext	This specification is used to state the complete file name with its corresponding extension.
`Instructions / Examples`	Examples of an application. e.g., • specifying memory partitions • processing a script • .....
Reference	Cross-reference to another section, figure or table.

Table 1: Terms and conventions

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1.3 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system was switched off. Violation of this guideline may result in damage / destruction of the module and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing and use ESD-safe tools, packing materials etc. and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

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2. Brief description

The TQM8315M is a universal microprocessor module based on Freescale's PowerPC CPU MPC8315(E). It is the first module in the new format 70 × 50 mm, and extends the spectrum of the Power architecture modules towards "low cost".

The performance of the used PowerQUICC II Pro (MPC83xx) is situated between PowerQUICC II (MPC82xx, TQM82xx modules) and PowerQUICC III (MPC85xx, TQM85xx modules).

In comparison to the TQM8349L it offers the following additional features:

- DDR2 instead of DDR-SDRAM
- 2 SERDES configurable as PCI Express ×1 or SGMII
- 2 SERDES as SATA

There are also some functional restrictions:

- Clock frequency e300-core max. 400 MHz
- Only 1 PCI interface (32 bit, 66 MHz)
- DDR2-SDRAM interface only 32 bit wide
- Local data bus only 16 bit wide

The Starterkit STK85xxNG is used as an Evaluation board for the TQM8315M. An additional adaptor STK-ECORE is available.

All function relevant pins of the microprocessor are led through to the module plug connectors. There are therefore no restrictions for customers using a module with respect to an integrated customised design.

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3. Technical data

3.1 Overview

3.1.1 Block diagram module

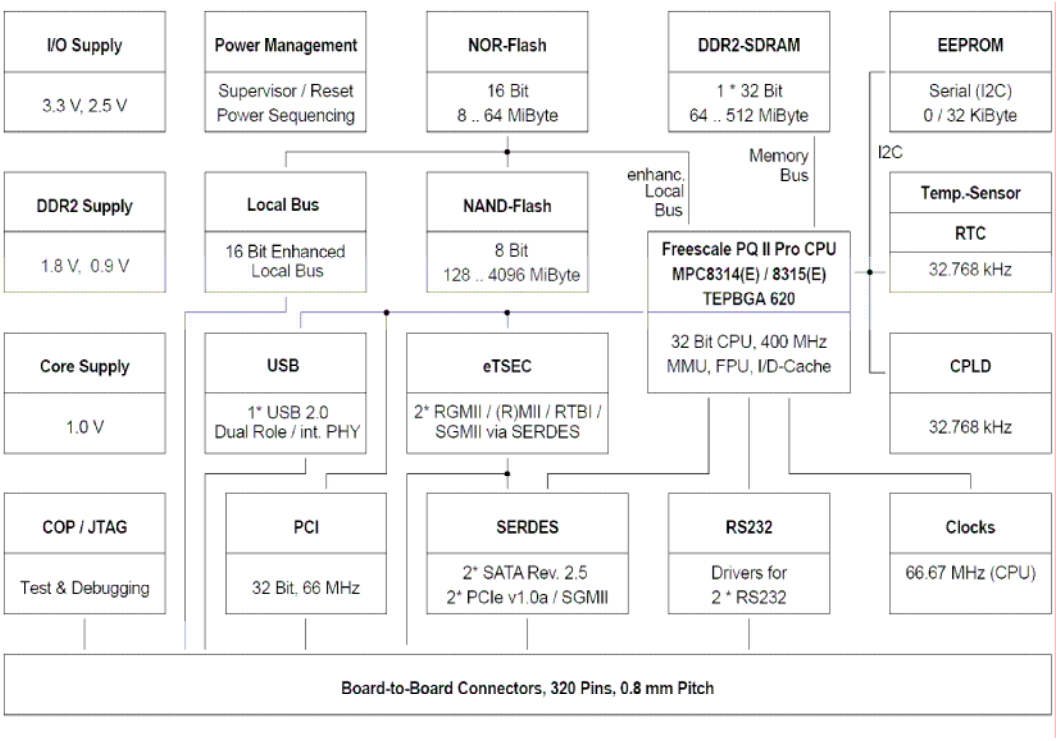

Illustration 1: Block diagram module

3.1.2 System components

- CPU MPC8315(E), MPC8314(E)
- Oscillator for CPU clock
- Reset generator / power fail logic and power sequencing
- CPLD for reset configuration
- Voltage regulator for 3.3 V, 2.5 V, 1.8 V and core voltage VDD (1.0 V)
- DDR2-SDRAM
- NOR flash
- NAND flash
- Serial EEPROM
- RTC
- Temperature sensor
- RS232 driver for two serial interfaces
- COP/JTAG interface
- Board-to-Board connector system

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3.2 Electronics

3.2.1 CPU

Alternatively to the MPC8315(E) an MPC8314(E) can also be mounted on the same module, because its pins are a subset of the MPC8315(E). The MPC8315(E) differs from the MPC8314(E) with respect to the fact that it has no own SATA interface. If not explicitly stated differently, all applicable CPU derivatives are covered by the MPC8315E. This also counts for derivatives without E (for Encryption).

The MPC8315E offers a large number of interfaces. On account of the high data rates special attention has to be paid to the following interfaces:

3.2.1.1 Enhanced Three-Speed Ethernet Controller

Both Gigabit Ethernet interfaces of the MPC8315E are implemented via eTSECs.

All relevant pins are led through to the module plug connectors, so that all interface modes supported by the CPU can be used. For RF-technical reasons PHY and transformer have to be placed on the base board.

- MII mode
  - Maximum frequency to be transmitted: 25 MHz (Tx- and Rx clock @ 100 Mbit/s)
- RMII mode
  - Maximum frequency to be transmitted: 50 MHz (Tx- and Rx clock @ 100 Mbit/s)
  - Lower signal number than with MII
  - Timing tighter than with MII, because both clock edges are used
- RGMII-and RTBI mode
  - Maximum frequency to be transmitted 125 MHz (Tx- and Rx clock @ 1 Gbit/s)
  - Lower signal number than with (G)MII
  - Timing tighter than with (G)MII, because both clock edges are used

Note:

The GMII mode is not supported by the CPU [1].

3.2.1.2 Serializer/Deserializer

The SerDes controller can be operated as an SGMII or as a PCI Express:

- SGMII mode or PCI Express
- Maximum frequency to be transmitted: 625 MHz (SGMII) or 1.25 GHz (PCI Express)

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3.2.1.3 SATA

With the TQM8315M a SATA interface is implemented on a PowerQUICC module for the first time.

Both SATA controllers of the MPC8315E support SATA I (1.5 Gbit/s) and SATA II (3 Gbit/s) and are implemented in the CPU including both PHYs. The SATA interfaces don't transmit an own clock signal. Instead, the principle of the "embedded clock" with CDR (clock and data recovery) is used here. Because of the 8B/10B encoding the usable transfer rate is only 80 % of the bit rate, i.e. 150 Mbyte/s or 300 Mbyte/s.

Note:

The physical layer "External Applications" (eSATA) and „Long Backplane Applications " (Rev. 1.x and 2.x) are not supported by the MPC8315E [1].

3.2.2 Reset logic

The reset logic contains the following functions:

- Monitoring of the voltages used on the module as follows:
  - 3.3 V, 2.5 V, 1.8 V
  - VDD (core voltage)
  - VREF (reference voltage for DDR2-SDRAM)
- External reset input and a PGOOD output
- Display of the reset state by a LED (function: SRESET# low → LED lights up)

3.2.2.1 Tolerances and reset trigger level for VCC3V3

Tolerance range of the fed supply voltage:
VCC3V3ID = 3.201 … 3.465 V = 3.3 V –3 % / + 5 %

Permitted voltage range of CPU and 3.3 V logic:
VCC3V3 = 3.135 … 3.465 V

Tolerance of the voltage monitoring, voltage drop in VCC3V3 taken into consideration:
V_{Reset} = 3.135 … 3.201 V

Excess voltage monitoring is optionally possible.

3.2.2.2 Optional monitoring of VREF

The reference voltage VREF for DDR2 can be optionally monitored. The integrated monitoring device must be configured accordingly.

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3.2.2.3 Reset-LED

- LED is controlled via the HRESET#-Signal, HRESET# low → LED lights up
- The luminous duration of the LED is extended by approx. 100 ms to ensure the visibility with very short reset pulses, e.g., with an internal reset

3.2.2.4 JTAG-Reset

- TRST# must be pulled low by PORESET# when PORESET# is set low, but still be able to be triggered separately (COP/JTAG debugging)

The circuit implemtented on the module is shown in the following illustration:

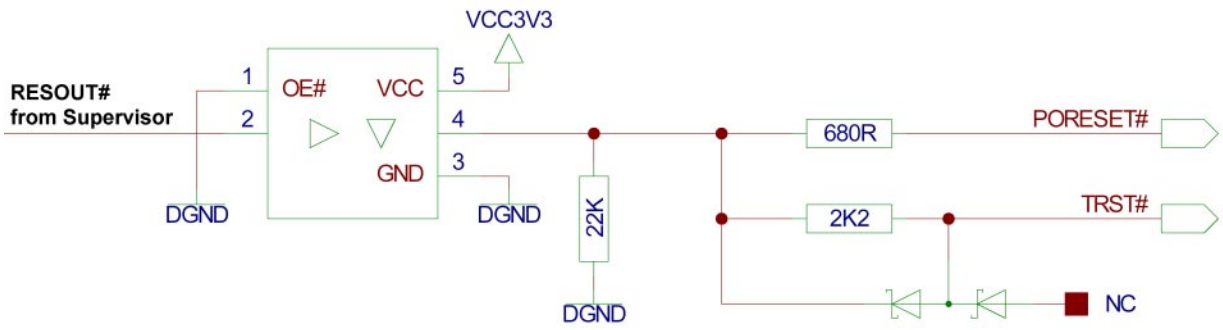

Illustration 2: Wiring of TRST# on the TQM8315M

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3.2.3 Reset configuration

3.2.3.1 Choice of the configuration source

- The encoded configuration information must be applied externally to the module pins (SEL_RESET_SOURCE and SEL_CLKIN_DIV)
- The PLD takes over and decodes the data
- The PLD supplies configuration signals CFG_RESET_SOURCE[0:3] and CFG_CLKIN_DIV as a function of HRESET# to the CPU

Module signal	CPU signal at reset	Configuration
SEL_CLKIN_DIV	**CFG_CLKIN_DIV**	
0 (Default)	0	CLKIN : PCI_SYNC_OUT = 1 : 1
1	1	CLKIN : PCI_SYNC_OUT = 2 : 1

Module signal	CPU signal at reset	Configuration	Boot Chip Select
SEL_RESET_SOURCE	**CFG_RESET_SOURCE[0:3]**		**LCS0#**
0	0b0000	NOR flash at the Local Bus	NOR flash
1 (Default)	0b0100	I²C-EEPROM	depending on configuration data ROMLOC[0:2]
Z	0b0101	NAND flash (large block) at the Local Bus State redefined compared to TQM8349L and TQM8360L!	NAND flash

Table 2: Configuration signals

3.2.3.2 Power-On reset configuration from I²C-EEPROM

- The configuration is simply alterable by the CPU, e.g., for the adaptation of TSEC modes
- The CPU prevents problems with a stuck I²C bus by automatically sending a special I²C bus reset sequence (not documented in [1])

3.2.3.3 Power-On reset configuration from NOR / NAND flash

- Alternative to reset configuration from I²C-EEPROM
- Updates are more difficult (only complete sectors of the flash can be deleted, reset configuration is stored in the same sector as the U-Boot or other boot loader)
- Possible use, e.g. for a default configuration (factory setting), if configuration data in the I²C-EEPROM is invalid
- The use of a reset configuration from flash only makes sense, if the boot process is performed from the concerning flash. Therefore the PLD switches the boot chip select to the respective flash (NOR or NAND), see Table 3.

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3.2.3.4 Detailed reset configuration

By updating the configuration-EEPROM all settings can be customised according to the requirements of the respective application. Table 3 shows the configurable settings of the CPU. The possible values are described in 4.2.

Reset configuration name	Register bit(s) meaning	Factory default*	Software writable
LBIUCM	Local Bus memory controller clock mode	0	–
DDRCM	DDR SDRAM memory controller clock mode	0	–
SVCOD	System PLL VCO division	0b01 / 4 → VCO freq = 533 MHz	–
SPMF[0:3]	System PLL Multiplication Factor	0b0010	–
COREPLL[0:6]	Core PLL Configuration	0b0000100 / 2 → VCO freq = 533 MHz	–
PCIHOST	PCI Host Mode	1	–
PCIARB	PCI Internal Arbiter mode	1	+
COREDIS	Core disable mode	0	–
BMS	Boot memory space	0	+
BOOTSEQ[0:1]	Boot Sequencer configuration	0b00	–
SWEN	Software watchdog enable	0	+**
ROMLOC[0:2]	Boot ROM interface location	0b110 (0b101)	–
RLEXT	Boot ROM location extension	0b00 (0b01)	–
TSEC1M	TSEC1 mode	0b011	
TSEC2M	TSEC2 mode	0b011	
TLE	True Little Endian	0	–
LALE	Local Bus LALE signal timing	0	–

Table 3: Configuration data CPU

* with configuration EEPROM as programmed by TQ
** writeable once after reset
+ = yes, – = no

3.2.3.5 Settings via the boot sequencer

The boot sequencer offers an additional possibility to configure the CPU without any support by the software. The boot sequencer is not linked to the reset configuration (detail see 4.2).

- Identical with the mechanism, which reads the reset configuration word from the I²C-EEPROM. Starts, however, only after the reset has ended
- Can partly replace / anticipate the configuration of the CPU by the software
- Application cases:
  - Multi processor environments
  - Preconfiguration to boot from other systems (e.g., PCI, SDRAM …)
  - Eliminating incompatibilities with reset values (e.g., bus driver control LBCTL)

Notes:

- Incorrect data can lead to an unbootable system!
- The boot software in combination with the Starterkit (or Starterkit plus start-up adaptor) should not be dependent on the boot sequencer

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3.2.4 PLD

The PLD fulfils the following tasks:

- Choice of the configuration source (see 3.2.3.1)
- Switch-over of boot chip select between NAND or NOR flash (see 3.2.3.3)

3.2.5 Clock

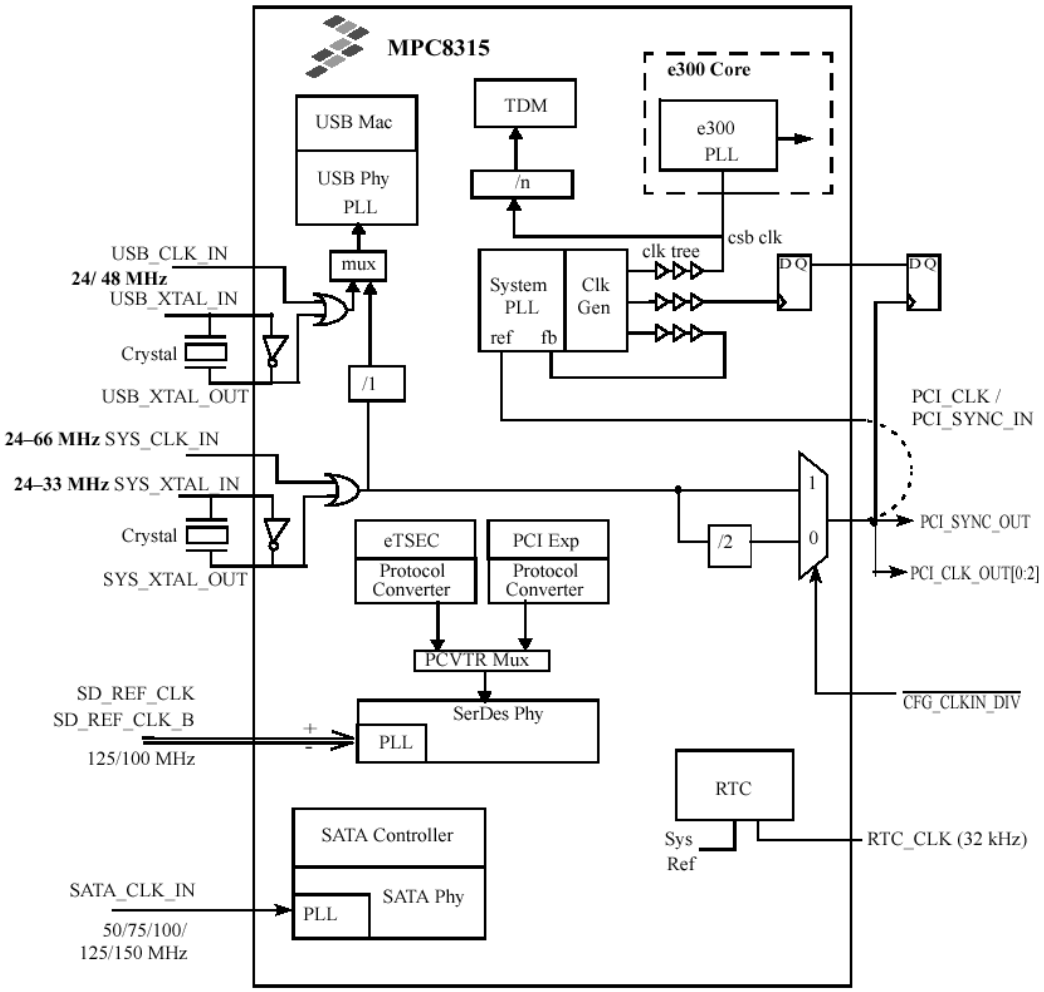

Illustration 3: Internal clock structure MPC8315E

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3.2.5.1 System Clocks

- When the CPU is PCI host, SYS_CLK_IN is the clock input. In this case a feedback of PCI_SYNC_OUT → PCI_SYNC_IN is necessary
  (to be implemented on the base board)
- Frequency leads 1 : 1 or divided 2 : 1 to all PCI clocks (see 3.2.5.2)
- PCI_SYNC_IN is the clock input if CPU is PCI agent
- On the module clocked with 66.6667 MHz, the internal clock is switchable to agent mode or external feed (signal CLKOE)
- Frequency range for external feed 24 … 66 MHz
- Slew rate of SYS_CLK_IN is specified with very close tolerances → for an external feed it is recommended to mount a driver NC7SV126 with a serial resistance of about 33 Ω very close to the module

The circuit implemtented on the module is shown in the following illustration:

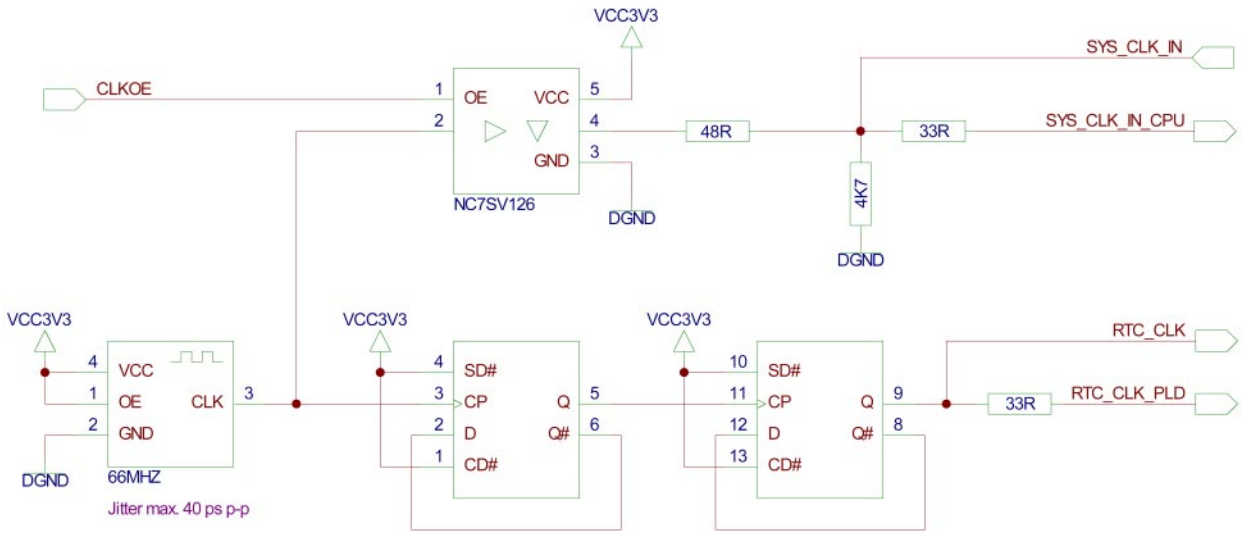

Illustration 4: Wiring of SYS_CLK_IN on the TQM8315M

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3.2.5.2 PCI Clocks

- Complex CLKIN / CFG_CLKIN_DIV / PCI_SYNC_OUT / PCI_CLK_OUT[0:2] is an integrated clock driver with PLL to balance signal run-times of the PCI clocks
- The reference is always PCI_SYNC_IN

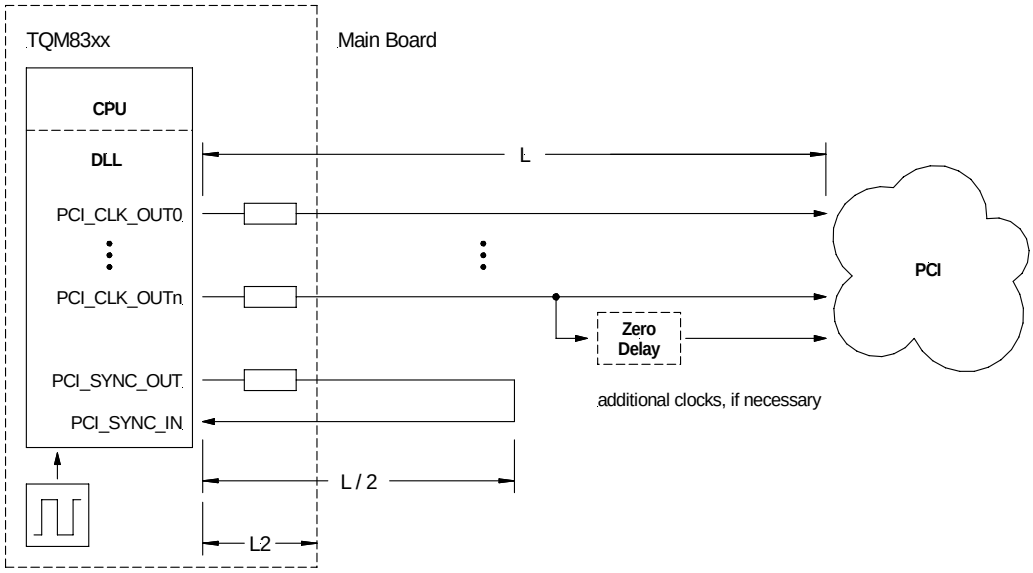

Illustration 5: Clock driver

All existing clock outputs PCI_CLK_OUT[0:2] are made externally available. If more subscribers than existing clock outputs have to be supplied, an additional zero delay buffer has to be provided on the base board.

If PCI is not used, the length of the return wiring (not the return itself!) is meaningless.

For the operation as a PCI agent the clock generator can be switched off (according to PCI spec at constant low level). Then the PCI clock is fed from external to PCI_SYNC_IN. In this mode of operation the base board is exclusively responsible for the clock distribution. In this mode of operation the outputs PCI_CLK_OUT[0:2] are not usable. The specification of the supplied signal can be looked up in the specification of the CPU [2].

3.2.5.3 Coherent System Bus Clock

- Is generated by multiplication of the clock input (SYS_CLKIN or PCI_CLK) (Multiplication factor is defined by reset configuration)
- Available as a CPU-internal signal only
- Used for DDR2-SDRAM, Local Bus and CPU-internal
- Frequencies:
  - 100, 133 MHz (with SYS_CLKIN = 33.33 MHz) [1]
  - 133 MHz (with SYS_CLKIN = 66.67 MHz) [1]

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3.2.5.4 Processor Core Clock

- Is generated by multiplication of CSB_CLK
  (Multiplication factor is defined by reset configuration)
- Available as a CPU-internal signal only
- Used for e300 core
- Frequencies: 133, 200, 266, 333, 400 MHz (with CSB_CLK = 133 MHz) [1]

3.2.5.5 Local Bus Clock

- Is generated from CSB_CLK
  (factor 1 or 2 is defined by reset configuration bit LBIUCM)
- Used for Local Bus
- Configurable at run-time via LCRR[CLKDIV] (division by 2 / 4 / 8)
- Frequencies: 16 / 33 / 66 MHz (with CSB_CLK = 133 MHz) [1]

3.2.5.6 Memory Bus Clock

- Is generated from CSB_CLK
  (factor 1 or 2 is defined by reset configuration bit DDRCM)
- Used for DDR-SDRAM (= frequency MCKx = half data rate)
- Frequency range: 125 … 133 MHz minimal frequency is determined by DDR2 [1]

3.2.5.7 Real Time Clock

- Independent clock input for CPU-internal time base
- Is always fed with 16.6667 MHz regardless of all other CPU clocks
- Allows as a reference clock the determination of own clock frequency
- Time base is no substitute for a real RTC, because of no possibility for buffering

3.2.5.8 USB Clock

- Used for internal USB-PHY
  (in contrast, USB controller runs synchronically with CSB_CLK/1, /2 or /3)
- Stable clock frequency 24 or 48 MHz necessary, choice via CONTROL[CLKIN_SEL]
- USB_CLK_IN must be fed externally. The specification of the supplied signal can be looked up in the specification of the CPU [2].

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3.2.5.9 SERDES Clocks

- Used for SERDES interfaces and the thereby implemented protocols PCIe, SGMII and SATA
- Possible clock frequencies if used as PCIe or SGMII: 100 MHz or 125 MHz
- Possible clock frequencies if used as SATA:
  MPC8315E: 50, 75, 100, 125 or 150 MHz single ended → low clock frequency advantageous
- Allowed jitter max. 100 ps cycle-to-cycle, concerning other specification of the supplied signal please refer to the specification of the CPU [2].
- Must be fed externally (reference circuits see STK-ECORE)
  - Possibility 1: ground-related feed (standard)
  - Possibility 2: differential feed
    - SATA RefClk compatibility option inevitable on module
    - Advantage: forward compatibility with future modules with differential reference clock

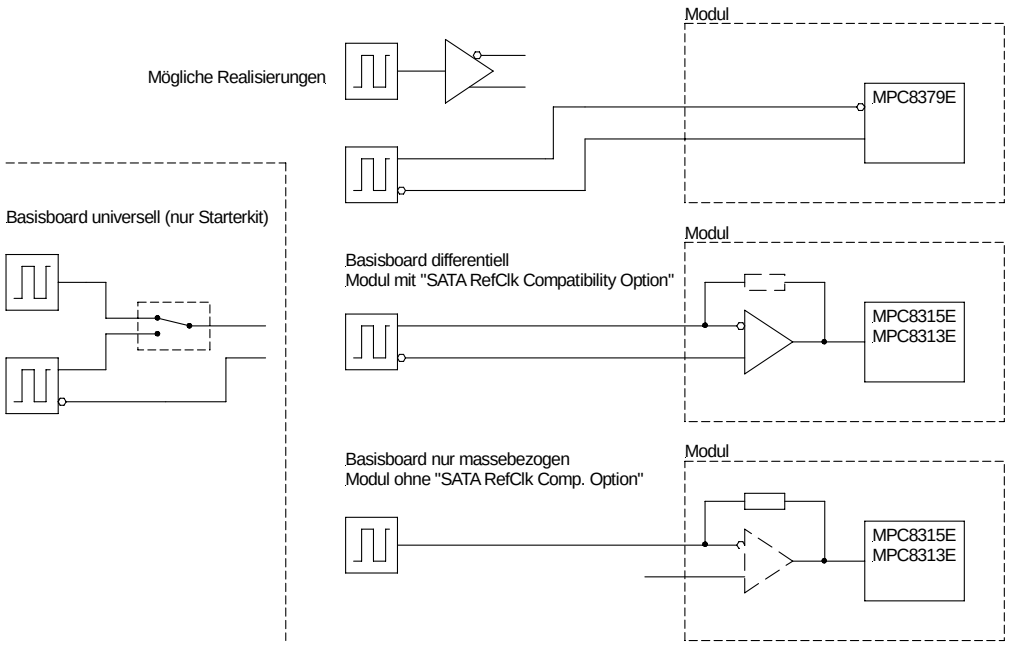

Illustration 6: SATA RefClk compatibility option

3.2.5.10 Overview standard clock rates

Clock	Frequency [MHz]	Remarks
SYSCLK	66.6667	
PCI_CLK	33 / 66	From SYSCLK, if applicable divided internally
CSB_CLK	267	
CORE_CLK	400	
LCLK	33 / 66	Standard frequency underlined
MCK * 2	267	= Data rate
RTC/PIT_CLK	16.6667	SYSCLK / 4
USB_CLKIN	48	When required externally

Table 4: Standard clock rates

3.2.6 Local Bus

The available chip selects are associated as follows:

Chip select	Usage on TQM8315M
LCS0#	NOR- / NAND flash 1 (Boot)
LCS1#	NOR- / NAND flash 1
LCS2#	Unused
LCS3#	NAND flash 2*

Table 5: Assignment chip selects at the Local Bus

* depending on used NAND device, if applicable freely

Depending on the choice of boot source LCS0# and LCS1# are exchanged in the module, to boot via LCS0# (boot chip select) alternatively from NOR or NAND flash. This exchange is done by the PLD as a function of the configuration source and if applicable, of the configuration data, see Table 3.

3.2.7 NOR flash

- 3.3 V flash of Micron's Strata-Flash-P33 series, 16 bit wide
- Connected to the Local Bus via a latch, due to multiplexed address / data
- 1 bank with 16 bit bus width
- 8 Mbyte to 64 Mbyte
- Access time 95 ns
- Chip select LCS0#, if booting from NOR flash, else exchange with LCS1# (NAND flash 1)

As the status signal WAIT of the flashes is not used by the CPU, i.e. the execution of the write cycles and the delete cycles must be monitored by polling.

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3.2.8 NAND flash

- NAND flash 1 × 8 bit wide, TSOP48, 3.3 V
- Connected to the Local Bus without buffer
- Component placement possibility from 1 to 32 Gbit
  (ask for available expansion stages)
- Single Level Cell (SLC), due to higher reliability than Multi Level Cell (MLC)
- Max. 2 chip selects (see 3.2.6)
- Status line R/B# of the flashes buffered with open collector driver

Note:

NAND Flash devices have an extremely short life cycle. This must be countered with appropriate measures (stock-keeping, qualification of follow-up devices, ...). Concerning this issue please contact your sales representative of TQ-Components.

Signal NAND flash	TQM8315M, via FCM
Chip Select	LCS3#
Command Latch Enable	LFCLE / LGPL0
Address Latch Enable	LFALE / LGPL1
Write Enable	LFWE# / LBS#
Read Enable	LFRE# / LGPL2
Ready / Busy	LFRB# / LGPL3
Write Protect	LFWP# / LGPL3

Table 6: Control signals

3.2.9 DDR2-SDRAM

- DDR2-SDRAMs, 32 bit wide
- Synchronous dynamic RAM, double data rate
- 64 … 512 Mbyte
- Max. 133 MHz clock (DDR2-266)
- Strobes single ended
- 1 memory bank with 32-bit width
- Serial termination
- Chip select MCS0# (stacked DDR is not planned)
- BGA package (84 or 92 balls)

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3.2.10 I²C Devices

All I²C bus devices on the module are connected to the I²C controller of the CPU. The used addresses are shown in the following table.

Device	MSB							LSB
Data EEPROM	1	0	1	0	1 (A2)	1 (A1)	1 (A0)	R/W
Configuration EEPROM	1	0	1	0	0 (A2)	0 (A1)	0 (A0)	R/W
Real Time Clock	1	1	0	1	0	0	0	R/W
Temperature Sensor	1	0	0	1	0 (A2)	0 (A1)	0 (A0)	R/W
Power Manager	1	0	0	0	1	0 (A1)	0 (A0)	R/W

Table 7: IIC1 device addresses

Note:

The signals IIC_SCL and IIC_SDA have each a 2.4 kΩ pull-up. These pull-ups on the module are sufficient for the bus load on the module. In case more bus loads are added, additional pull-ups have to be switched in parallel to achieve adequate falling and rising edges.

3.2.10.1 Data EEPROM

The serial EEPROM can store, e.g., characteristics of the module and customer specific parameter data. In the EEPROM single memory cells can be deleted and be overwritten in contrast to flash. At delivery the EEPROM is erased. It can, e.g., save application parameters non-volatile.

- 0 or 32 kbyte
- Possible I²C clock frequency 400 kHz
- Is freely available for user's data
- Control via I²C controller IIC1, device address see Table 7

3.2.10.2 Configuration-EEPROM

At delivery the configuration-EEPROM contains a standard reset configuration (see 3.2.3.4).

- 4 kbyte
- Possible I²C clock frequency 400 kHz
- Used for reset configuration
- Update by the CPU is possible
- Control via I²C controller IIC1, device address see Table 7

Note:

Changes might lead to an inoperative system. In this case the recovery of a functional reset configuration is only possible by an external master (programmer) at the I²C bus. A suitable tool can be advised by the support of TQ-Components.

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3.2.10.3 RTC

Because there is no CPU-internal bufferable RTC, the RTC was implemented externally:

- RTC DS1337U, control via I²C bus of the CPU
- Possible I²C clock frequency 400 kHz
- Battery buffering possible (battery on base board)
- Alarm outputs INTA# and SQW/INTB# (open drain) connected to common pin
- Control via I²C controller IIC1, device address see Table 7
- Quartz tolerance 30 ppm

3.2.10.4 Temperature monitoring

- Is placed near the CPU for indirect monitoring of the CPU temperature
- Sensor LM75
- Possible I²C clock frequency 400 kHz
- Switch output of the LM75 led out
- Control via I²C controller IIC1, device address see Table 7

3.2.11 General-Purpose-I/O

- A total of 32 GPIOs, implemented as GPIO[0:31]
- 24 of these GPIO signals are multiplexed with other interface and control signals, e.g., TSEC, USB, GTM, DMA
- Configured as inputs after Power-On-reset
- Open drain capable
- Interruptible

3.3 Supply

The following voltages exist on the module:

Voltage	Usage
3.3 V	CPU (Local Bus, PCI, eTSEC) NOR and NAND flash RTC, I²C -EEPROM, CPLD, other logic
2.5 V	CPU (if applicable eTSEC)
1.8 V	CPU (DDR2) DDR2-SDRAM
1.0 V	CPU (core), SERDES (SATA, PCIe, SGMII)
0.9 V	DDR2-SDRAM reference voltage

Table 8: Supply voltages internal

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3.3.1 Power supply possibilities

The module is supplied exclusively with 3.3 V. All other voltages are generated on the module from this. To achieve a valid power sequencing, 3.3 V are switched on the module.
The supply encloses the following function blocks:

- Switch for 3.3 V
- Regulator from 3.3 V to 2.5 V (voltage for eTSEC-I/Os)
- Step-down switching regulator from 3.3 V to 1.8 V (voltage for DDR2-SDRAMs)
- Step-down switching regulator from 3.3 V to 1.0 V (core voltage)

The supply structure is shown in Illustration 7:

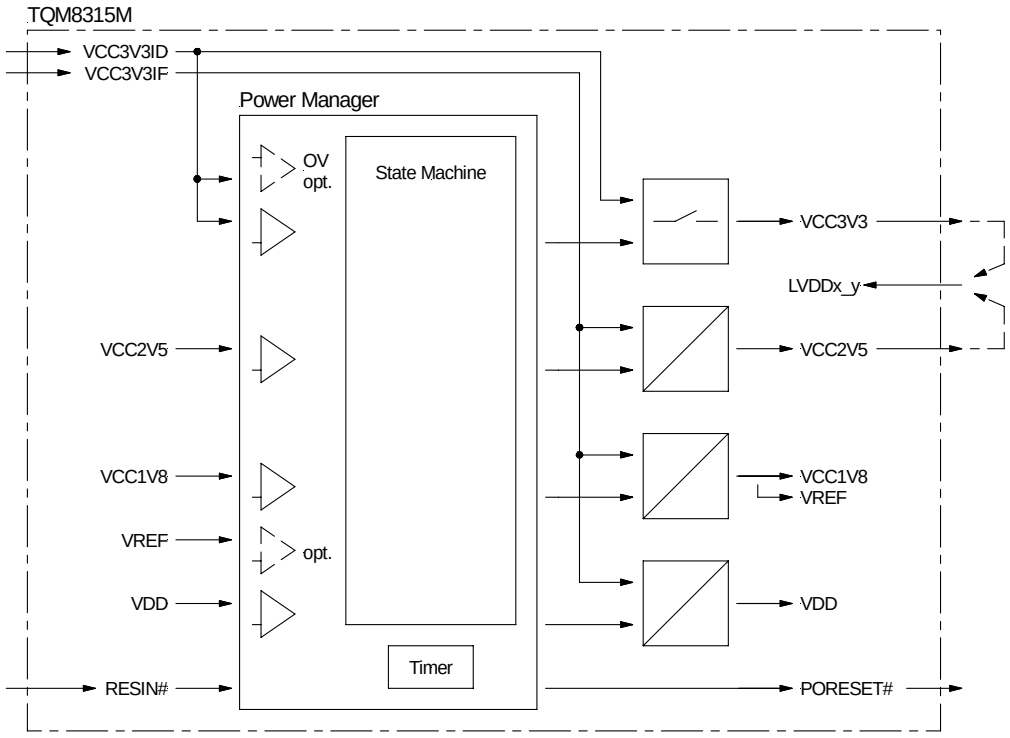

Illustration 7: Supply structure

Maximum ratings for the supply voltages to be fed:

Voltages VCC3V3IF and VCC3V3ID	3.201 … 3.465 V	Determined by voltage range of components and supervisor threshold (see 3.2.2.1)
Max. ripple	30 mV	Peak to peak
Current consumption	1.7 A	TQM8315M @ 400/267 MHz (core/DDR)

Table 9: Requirements for 3.3 V external

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3.3.2 Power sequencing

- The power sequencing is implemented by an integrated power management device, see Illustration 7, ensuring a high flexibility
- As recommended in the specification of the MPC8315E, the core voltage VDD is booted up first (thereby, PORESET# = low), before the other voltages are switched on. In this way undefined start-up conditions of the CPU should be avoided [1]
- In spite of this measure undefined start-up conditions may occur. This should be taken into consideration in the design of the base board if necessary. Especially vulnerable are non-volatile memories, e.g., the chip select for a battery-buffered RAM

3.3.3 RTC supply VBAT

- Supply of the RTC
- Current consumption only, if VBAT > VCC3V3
  (connection to VCC3V3 via Schottky diode present on module)

Voltage VBAT	1.8 … 5.5 V	Determined by voltage range of RTC (see 3.2.10.3)
Max. ripple	1 %	Peak to peak
Timekeeping current	2 µA	VCC3V3IF = VCC3V3ID = 0 V, oscillator running

3.3.4 3.3 V supply

- Main supply of the module, 3.3 V
- Switchable for power sequencing
- Led through for application-specific supply of LVDD1_OFF and LVDD2_ON, cf. Illustration 7
- In addition, no current drain (e.g., for the supply of external devices) allowed

3.3.5 2.5 V supply

- 2.5 V exclusively to the application-specific supply of 2.5 V peripheral in LVDD1_OFF and LVDD2_ON, cf. Illustration 7
- In addition, no current drain (e.g., for the supply of external devices) allowed

3.3.6 Supply Ethernet-I/O

- 2.5 or 3.3 V, depending on the use of the interfaces supplied by it
- Determined by connection on base board of LVDD1_OFF or LVDD2_ON to VCC3V3 or VCC2V5 to LVDDx_y, see Illustration 7

3.3.7 Reference voltage VREF

- Reference voltage 0.9 V for DDR2-SDRAMs
- Monitoring is optionally possible; can be configured suitable by adapting the configuration of the power management device

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3.3.8 VDD supply

- Voltage 1.0 V
- Core voltage of the CPU

3.4 Interfaces to other systems and devices

3.4.1 Serial interfaces

- Two internal UARTs: UART0, UART1
- Max. 115200 baud (limited by driver / level converter)
- Driver with RS232 compatible levels
- All signals also available without driver
- Default assembly is a driver with 2 × RxD / TxD

3.4.2 COP/JTAG interface

All lines of the Freescale COP/JTAG interface (debugging interface) are made available externally. Like the TQS-debugging interface, the COP/JTAG interface is also exclusively led through to the connectors on the base board.

The COP/JTAG interface incorporates the following signals
(signal direction seen from the module respective the Starterkit)

Pin*	Signal name	Type	Function
1	TDO	O	Test Data Output
3	TDI	I/O	Test Data Input
9	TMS	I/O	Test Mode Select
7	TCK	O	Test Clock
4	TRST#		Test Reset
5	NC	I	(Was QREQ# Quiescent Request)
12	NC	–	(Was GND Ground)
11	SRESET#	I	Soft Reset
13	RESIN#	I	Reset In *
15	CKSTP_OUT#		Check Stop Out
16	GND	–	Ground
6	VDD_SENSE	O	(Was 3.3 V)

Table 10: Signals COP/JTAG interface

* on Starterkit STK85xxNG

The wiring can also be taken from the circuit diagram of the STK85xxNG.

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3.4.3 External bus / other interfaces

The interfaces described here are led through to the two 160-pin plug connectors leading to the base board.

3.4.3.1 Treatment of unused pins

The module was designed in such a way, that only a minimum number of signals are necessary for the operation. Hence, many signals do not need external wiring if their function is not required.

- Pure outputs (type = O): No wiring necessary
- Inputs and I/Os with pull-up / pull-down (type = O, I/O, pull-up or pull-down is described): No wiring necessary
- I/Os which can be configured as an output (GPIO1[x], GPIO2[x]): In general it is sufficient to configure unused pins as an output during initialization
- Further notes are found in [2]

3.4.3.2 Pinout according to function groups

Signal	CPU pin	Type	Description	Module pin
GPIO / TDM				
GPIO_18 / TDM_RCK	AB1	I/O	General-purpose I/O signal 18 / TDM receive clock	X1-78
GPIO_19 / TDM_RFS	AB3	I/O	General-purpose I/O signal 19 / TDM receive frame sync	X1-79
GPIO_20 / TDM_RD	AC1	I/O	General-purpose I/O signal 20 / TDM receive data	X1-80
GPIO_21 / TDM_TCK	AB5	I/O	General-purpose I/O signal 21 / TDM transmit clock	X1-83
GPIO_22 / TDM_TFS	AC2	I/O	General-purpose I/O signal 22 / TDM transmit frame sync	X1-84
GPIO_23 / TDM_TD	AC3	I/O	General-purpose I/O signal 23 / TDM transmit data	X1-85
GPIO / DMA / Timer				
GPIO_0 / DMA_DREQ1# / GTM1_TOUT1#	C5	I/O	General-purpose I/O signal 0 / DMA request 1 / Timer out 1	X1-86
GPIO_1 / DMA_DACK1# / GTM1_TIN2 / GTM2_TIN1	A4	I/O	General-purpose I/O signal 1 / DMA acknowledge 1 / Timer in 1/2 Timer in 2/1	X1-87
GPIO_2 / DMA_DONE1 / GTM1_TGATE2# / GTM2_TGATE1#	K3	I/O	General-purpose I/O signal 2 / DMA done 1 / Timer gate 1/2 / Timer gate 2/1	X1-88

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Signal	CPU pin	Type	Description	Module pin
GPIO / DMA / Timer				
GPIO_3 / GTM1_TIN3 / GTM2_TIN4	K1	I/O	General-purpose I/O signal 3 / Timer in 1/3 / Timer in 2/4	X1-89
GPIO_4 / GTM1_TGATE3# / GTM2_TGATE4#	K2	I/O	General-purpose I/O signal 4 / Timer in 1/3 / Timer in 2/4	X1-90
GPIO_5 / GTM1_TOUT3# / GTM2_TOUT1#	L5	I/O	General-purpose I/O signal 5 / Timer out 1/3 / Timer out 2/1	X1-91
GPIO_6 / GTM1_TIN4 / GTM2_TIN3	L3	I/O	General-purpose I/O signal 6 / Timer in 1/4 / Timer in 2/3	X1-92
GPIO_7 / GTM1_TGATE4# / GTM2_TGATE3#	L1	I/O	General-purpose I/O signal 7 / Timer gate 1/4 / Timer gate 2/3	X1-95
DMA_DREQ0# / GPIO_12	AD1	I/O	DMA request 0 / General-purpose I/O signal 12	X1-75
DMA_DACK0# / GPIO_13	AC4	I/O	DMA acknowledge 0 / General-purpose I/O signal 13	X1-76
DMA_DONE0# / GPIO_14	AD2	I/O	DMA done 0 / General-purpose I/O signal 14	X1-77
USB				
USB_VBUS	C12	I	USB 2.0 VBUS line	X1-109
USB_CLK_IN	B15	I	USB clock input	X1-96
GPIO_8 / USBDR_DRIVE_VBUS / GTM1_TIN1 / GTM2_TIN2	M1	I/O	General-purpose I/O signal 8 / USB Vbus power enable / Timer in 1/1 / Timer in 2/2	X1-99
USB_DM	A12	I/O	USB 2.0 D- line	X1-108
USB_DP	A11	I/O	USB 2.0 D+ line	X1.110
GPIO_9 / USBDR_PWRFAULT / GTM1_TGATE1# / GTM2_TGATE2#	M2	I/O	General-purpose I/O signal 9 / USB Vbus power fault / Timer gate 1/1 / Timer gate 2/2	X1-101
GPIO_11 / USBDR_PCTL1 / GTM1_TOUT4# / GTM2_TOUT3#	M4	I/O	General-purpose I/O signal 11 / USB Port control 1 / Timer out 1/4 / Timer out 2/3	X1-105
GPIO_10 / USBDR_PCTL0 / GTM1_TOUT2# / GTM2_T OUT1#	M5	I/O	General-purpose I/O signal 10 / USB Port control 0 / Timer out 1/2 / Timer out 2/1	X1-103

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Signal	CPU pin	Type	Description	Module pin
Debug / Test				
TCK	E5	I	Test clock	X1-26
TDI	B4	I	Test data in	X1-19
TMS	C3	I	Test mode select	X1-25
TRST#	C2	I	Test reset	X1-27
TDO	C4	O	Test data out	X1-20
TEST_MODE	D6	I	Signal is tied to DGND	X1-38
Interrupt Controller / DMA				
IRQ[7] / CKSTOP_IN#	AA5	I	External interrupt 7 / Check Stop In	X1-34
IRQ[5] / CORE_SRESET_IN#	AA2	I	External interrupt 5 / Core Soft Reset In	X1-32
IRQ[3]	AA1	I	External interrupt 3	X1-30
IRQ[1]	E1	I	External interrupt 1	X1-28
IRQ[6] / CKSTOP_OUT#	AA4	I/O	External interrupt 6 / Check Stop Out	X1-35
IRQ[4]	Y5	I	External interrupt 4	X1-33
IRQ[2]	A7	I	External interrupt 2	X1-31
IRQ[0] / MCP_IN#	Y3	I	External interrupt 0 / Interrupt Request Output	X1-29
Clocks				
SYS_CLK_IN	K28	I	Clock input	X1-72
RTC_CLOCK	K26	I	Timer clock, real time clock	X1-70
PCI_CLK0	E23	O	PCI clock 0	X2-43
PCI_CLK1	F24	O	PCI clock 1	X2-46
PCI_CLK2	E25	O	PCI clock 2	X2-45
PCI_SYNC_IN	K27	I	PCI clock sync input	X2-47
PCI_SYNC_OUT	J27	O	PCI clock sync output	X2-48
I²C				
IIC_SCL / CKSTOP_IN#	N2	I/O	I²C serial clock / Check Stop In	X1-62
IIC_SDA / CKSTOP_OUT#	N1	I/O	I²C serial data / Check Stop Out	X1-63
Reset				
HRESET#	B6	I/O	Hard reset	X1-12
QUIESCE#	B5	O	Quiescent state	X1-14
PORESET#	A6	O	Power on reset	X1-11

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Signal	CPU pin	Type	Description	Module pin
SPI				
SPISEL / GPIO_17	W2	I/O	SPI slave select / General-purpose I/O signal 17	X1-69
SPIMOSI / GPIO_15	W3	I/O	SPI master-out slave-in / General-purpose I/O signal 15	X1-66
SPIMISO / GPIO_16	W4	I/O	SPI master-in slave-out / General-purpose I/O signal 16	X1-67
SPICLK	Y1	I/O	SPI clock	X1-71
MCP_OUT#	W1	O	Machine check interrupt output	X1-39
RS232 (via Transceiver)				
SIN2		I	Serial In Data 2, RS232 level	X1-48
SIN1		I	Serial In Data 1, RS232 level	X1-47
SOUT2		O	Serial Out Data 2, RS232 level	X1-50
SOUT1		O	Serial Out Data 1, RS232 level	X1-49
UARTs				
UART_CTS[2]	A17	I	DUART clear to send 2	X1-60
UART_CTS1# / MSRCID[2] / LSRCID[2]	D16	I/O	DUART clear to send 1 / Memory debug source ID 2 / LBC debug source port ID 2	X1-59
UART_SOUT2 / MSRCID[4] / LSRCID[4]	A16	O	DUART data serial out 2 / Memory debug source ID 4 / LBC debug source port ID 4	X1-56
UART_SOUT1# / MSRCID[0] / LSRCID[0]	C15	O	DUART data serial out 1 / Memory debug source ID 0 / LBC debug source port ID 0	X1-55
UART_RTS1# / MSRCID[3] / LSRCID[3]	B17	O	DUART ready to send 1 / Memory debug source ID 3 / LBC debug source port ID 3	X1-57
UART_SIN2 / MDVAL / LDVAL	C16	I/O	DUART serial data in 2 / Memory debug data valid / LBC debug data valid	X1-54
UART_SIN1# / MSRCID[1] / LSRCID[1]	B16	I/O	DUART serial data in 1 / Memory debug source ID 1 / LBC debug source port ID 1	X1-53
UART_RTS[2]	A18	O	DUART ready to send 2	X1-58
PCI1 / PCI-X / PCI 64 Bit				
PCI_AD[31]	B19	I/O	PCI address/data 31	X2-90
PCI_AD[30]	A21	I/O	PCI address/data 30	X2-86
PCI_AD[28]	D19	I/O	PCI address/data 28	X2-82
PCI_AD[29]	A19	I/O	PCI address/data 29	X2-84
PCI_AD[26]	C20	I/O	PCI address/data 26	X2-78
PCI_AD[27]	B21	I/O	PCI address/data 27	X2-80
PCI_AD[24]	E19	I/O	PCI address/data 24	X2-72

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Signal	CPU pin	Type	Description	Module pin
PCI1 / PCI-X / PCI 64 Bit				
PCI_AD[25]	A22	I/O	PCI address/data 25	X2-74
PCI_AD[23]	C22	I/O	PCI address/data 23	X2-70
PCI_AD[22]	A23	I/O	PCI address/data 22	X2-68
PCI_AD[21]	E20	I/O	PCI address/data 21	X2-66
PCI_AD[20]	A26	I/O	PCI address/data 20	X2-62
PCI_AD[18]	B26	I/O	PCI address/data 18	X2-58
PCI_AD[19]	C24	I/O	PCI address/data 19	X2-60
PCI_AD[16]	B25	I/O	PCI address/data 16	X2-54
PCI_AD[17]	D24	I/O	PCI address/data 17	X2-56
PCI_AD[14]	D28	I/O	PCI address/data 14	X2-83
PCI_AD[15]	D27	I/O	PCI address/data 15	X2-85
PCI_AD[13]	E28	I/O	PCI address/data 13	X2-81
PCI_AD[12]	E27	I/O	PCI address/data 12	X2-79
PCI_AD[11]	F27	I/O	PCI address/data 11	X2-77
PCI_AD[10]	G25	I/O	PCI address/data 10	X2-73
PCI_AD[8]	F26	I/O	PCI address/data 8	X2-69
PCI_AD[9]	F28	I/O	PCI address/data 9	X2-71
PCI_AD[6]	G27	I/O	PCI address/data 6	X2-65
PCI_AD[7]	G28	I/O	PCI address/data 7	X2-67
PCI_AD[4]	H28	I/O	PCI address/data 4	X2-59
PCI_AD[5]	H26	I/O	PCI address/data 5	X2-61
PCI_AD[3]	H27	I/O	PCI address/data 3	X2-57
PCI_AD[2]	K24	I/O	PCI address/data 2	X2-55
PCI_AD[1]	J24	I/O	PCI address/data 1	X2-53
PCI_AD[0]	J25	I/O	PCI address/data 0	X2-51
PCI_PAR	G24	I/O	PCI parity	X2-89
PCI_FRAME#	C28	I/O	PCI frame	X2-109
PCI_TRDY#	A24	I/O	PCI target ready	X2-115
PCI_IRDY#	D25	I/O	PCI initiator ready	X2-113
PCI_STOP#	D23	I/O	PCI stop	X2-92
PCI_IDSEL	D26	I	PCI initial device select	X2-96
PCI_DEVSEL#	E22	I/O	PCI device select	X2-94
PCI_PERR#	D21	I/O	PCI parity error	X2-104
PCI_SERR#	C25	I/O	PCI system error	X2-98
PCI_C/BE[3]#	E21	I/O	PCI command/byte enable 3	X2-107
PCI_C/BE[2]#	A25	I/O	PCI command/byte enable 2	X2-105
PCI_C/BE[1]#	C27	I/O	PCI command/byte enable 1	X2-97
PCI_C/BE[0]#	H24	I/O	PCI command/byte enable 0	X2-95

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Signal	CPU pin	Type	Description	Module pin
PCI1 / PCI-X / PCI 64 Bit				
PCI_PME#	B23	I/O	PCI PME assertion request	X2-50
PCI_GNT1# / CPCI_HS_LED	D17	O	PCI grant 1 / CompactPCI hot swap LED	X2-116
PCI_GNT2# / CPCI_HS_ENUM	E15	O	PCI grant 2 / CompactPCI hot swap enumerator	X2-118
PCI_GNT0#	B20	I/O	PCI grant 0	X2-114
PCI_REQ2#	E17	I	PCI request 2	X2-110
PCI_REQ1# / CPCI_HS_ES	C18	I	PCI request 1 / CompactPCI hot swap ejector switch	X2-108
PCI_REQ0#	E18	I/O	PCI request 0	X2-106
M66EN	L24	I	66-MHz system configuration	X2-2
PCI_INTA#	B18	O	PCI interrupt output	X2-91
PCI_RESET_OUT#	A20	O	PCI reset out	X2-93
EXT_PWR_CTRL	D3	O	External power control	X1-16
PMC_PWR_OK	D4	I	Stable power	X1-15
Local Bus				
LBCTL	AH26	O	LBC data buffer control	X1-111
LGPL5	AF22	O	LBC GP line 5	X1-124
LGPL4 / LGTA# / LUPWAIT / LFRB#	AA26	I/O	LBC GP line 4 / GPCM terminate access / UPM wait / Local Bus flash ready busy	X1-123
LGPL3 / LFWP#	Y24	O	LBC GP line 3 / Local Bus flash write protect	X1-122
LGPL2 / LOE# / LFRE#	Y25	O	LBC GP line 2 / LBC output enable / Local Bus flash read enable	X1-121
LGPL1 / LFALE	AA28	O	LBC GP line 1 / Local Bus address latch enable	X1-120
LGPL0 / LFCLE	Y27	O	LBC GP line 0 / Local Bus flash command latch enable	X1-119
LWE1#	AG26	O	LBC write enable 1	X1-115
LWE0# / LFWE0# / LBS#	AE23	O	LBC write enable 0 / Local Bus flash write enable 0 / Byte select	X1-113
LCS[3]#	AF24	O	LBC chip select 3	X1-128
LCS[2]#	AG24	O	LBC chip select 2	X1-127
LCS[1]#	AF25	O	LBC chip select 1	X1-126
LCS[0]	AD22	O	LBC chip select 0	X1-125
LA24	AH24	O	LBC port address 24	X1-139
LA22	Y28	O	LBC port address 22	X1-137

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Signal	CPU pin	Type	Description	Module pin
Local Bus				
LALE	AF26	O	LBC address latch enable	X1-114
LA25	AG23	O	LBC port address 25	X1-140
LA23	AH23	O	LBC port address 23	X1-138
LA21	W24	O	LBC port address 21	X1-136
LA19	W28	O	LBC port address 19	X1-134
LA17	V25	O	LBC port address 17	X1-132
LA20	U24	O	LBC port address 20	X1-135
LAD15	AD25	I/O	LBC address/data 15	X1-160
LAD13	AF28	I/O	LBC address/data 13	X1-158
LA18	W26	O	LBC port address 18	X1-133
LAD11	AE27	I/O	LBC address/data 11	X1-156
LA16	V24	O	LBC port address 16	X1-131
LAD9	AB24	I/O	LBC address/data 9	X1-152
LAD14	AC24	I/O	LBC address/data 14	X1-159
LAD12	AE26	I/O	LBC address/data 12	X1-157
LAD7	AC26	I/O	LBC address/data 7	X1-150
LAD10	AE28	I/O	LBC address/data 10	X1-155
LAD5	AD28	I/O	LBC address/data 5	X1-148
LAD8	AD27	I/O	LBC address/data 8	X1-151
LAD3	AA24	I/O	LBC address/data 3	X1-146
LAD6	AB25	I/O	LBC address/data 6	X1-149
LAD1	AB27	I/O	LBC address/data 1	X1-144
LAD4	AC27	I/O	LBC address/data 4	X1-147
LAD2	AC28	I/O	LBC address/data 2	X1-145
LAD0	AB28	I/O	LBC address/data 0	X1-143
LCLK0	AH25	O	LBC clock 0	X1-116
(e)TSECs1, 2				
GPIO_27 / TSEC2_CRS	E9	I/O	General-purpose I/O signal 27 / eTSEC2 carrier sense	X2-156
TSEC2_TX_ER	B11	O	eTSEC2 transmit error	X2-148
TSEC_GTX_CLK125	D1	I	Gigabit reference clock	X2-153
TSEC2_TX_EN	D12	O	eTSEC2 transmit enable	X2-146
TSEC2_RX_ER	A10	I	eTSEC2 receiver error	X2-132
TSEC2_GTX_CLK	B10	O	eTSEC2 transmit clock out	X2-154
TSEC2_RX_DV	C9	I	eTSEC2 receive data valid	X2-130
GPIO_26 / TSEC2_COL	A8	I/O	General-purpose I/O signal 26 / eTSEC2 collision detect	X2-158

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Signal	CPU pin	Type	Description	Module pin
(e)TSECs1, 2				
TSEC2_TXD[2] / CFG_RESET_SOURCE[1]	C7	I/O	eTSEC2 transmit data 2 / Reset configuration word source selection 1	X2-142
TSEC2_TXD[0] / CFG_RESET_SOURCE[3]	B7	I/O	eTSEC2 transmit data 0 / Reset configuration word source selection 3	X2-136
TSEC2_TXD[3] / CFG_RESET_SOURCE[0]	D11	I/O	eTSEC2 transmit data 3 / Reset configuration word source selection 0	X2-144
TSEC2_RX_CLK	B8	I	eTSEC2 receive clock	X2-134
TSEC2_TXD[1] / CFG_RESET_SOURCE[2]	E8	I/O	eTSEC2 transmit data 1 / Reset configuration word source selection 2	X2-140
TSEC2_TX_CLK	D8	I	eTSEC2 transmit clock in	X2-150
TSEC2_RXD[2]	D10	I	eTSEC2 receive data 2	X2-126
TSEC2_RXD[0]	B9	I	eTSEC2 receive data 0	X2-120
TSEC2_RXD[3]	C10	I	eTSEC2 receive data 3	X2-128
GPIO_25 / TSEC1_CRS / USBDR_TXDRXD1	H1	I/O	General-purpose I/O signal 25 / eTSEC11 carrier sense / USB data bit 1	X2-155
TSEC2_RXD[1]	A9	I	eTSEC2 receive data 1	X2-122
TSEC1_TX_ER / TSEC_TMR_ALARM2	G5	O	eTSEC1 transmit error / 1588 timer alarm-out 2	X2-145
GPIO_31 / TSEC1_TX_EN / TSEC_TMR_ALARM1	F4	I/O	General-purpose I/O signal 31 / eTSEC1 transmit enable / 1588 timer alarm-out 1	X2-143
GPIO_24 / TSEC1_COL / USBDR_TXDRXD0	J1	I/O	General-purpose I/O signal 24 / eTSEC1 collision detect / USB Data bit 0	X2-157
TSEC1_RX_ER / USBDR_DIR / TSEC_TMR_TRIG2	H5	I	eTSEC1 receiver error / USB Direction of data bus / 1588 trigger-in 2	X2-129
TSEC1_RX_DV / USBDR_TXDRXD4	J2	I/O	eTSEC1 receive data valid / USB Data bit 4	X2-127
GPIO_28 / TSEC1_TXD[3] / TSEC_TMR_GCLK	F3	I/O	General-purpose I/O signal 28 / eTSEC1 transmit data 3 / 1588 clock-out	X2-141
TSEC1_GTX_CLK / USBDR_TXDRXD2	K5	I/O	eTSEC1 transmit clock out / USB Data bit 2	X2-149
GPIO_30 / TSEC1_TXD[1] / TSEC_TMR_PP2	F1	I/O	General-purpose I/O signal 30 / eTSEC1 transmit data 1 / 1588 timer pulse-out 2	X2-135
TSEC1_TX_CLK / USBDR_CLK	G2	I	eTSEC1 transmit clock in / Clocking signal for ULPI PHY interface	X2-147
GPIO_29 / TSEC1_TXD[2] / TSEC_TMR_PP1	F2	I/O	General-purpose I/O signal 29 / eTSEC1 transmit data 2 / 1588 timer pulse-out 1	X2-139

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Signal	CPU pin	Type	Description	Module pin
(e)TSECs1, 2				
TSEC1_TXD[0] / USBDR_STP / TSEC_TMR_PP3	G4	O	eTSEC1 transmit data 0 / USB End of a transfer on the bus / 1588 timer pulse-out 3	X2-133
TSEC1_RXD[3] / USBDR_TXDRXD5	G1	I/O	eTSEC1 receive data 3 / USB Data bit 5	X2-125
TSEC1_RX_CLK / USBDR_TXDRXD3	J4	I/O	eTSEC1 receive clock / USB Data bit 3	X2-131
TSEC1_RXD[1] / USBDR_TXDRXD7 / TSEC_TMR_CLK	J5	I/O	eTSEC1 receive data 1 / USB Data bit 7 / 1588 clock-in	X2-119
TSEC_MDC	E3	O	Ethernet management data clock	X2-159
TSEC1_RXD[2] / USBDR_TXDRXD6	H3	I/O	eTSEC1 receive data 2 / USB Data bit 6	X2-121
TSEC_MDIO	E2	I/O	Ethernet management data in/out	X2-160
TSEC1_RXD[0] / USBDR_NXT / TSEC_TMR_TRIG1	H2	I	eTSEC1 receive data 0 / USB Next data / 1588 trigger-in 1	X2-117
SERDES				
PINRXPLUSA	M28	I	Receive plus A	X2-38
PINTXPLUSA	N25	O	Transmit plus A	X2-27
PINRXMINUSA	N28	I	Receive minus A	X2-42
PINTXMINUSA	M25	O	Transmit minus A	X2-31
PINRXPLUSB	T28	I	Receive plus B	X2-30
PINTXPLUSB	R26	O	Transmit plus B	X2-35
PINRXMINUSB	U28	I	Receive minus B	X2-34
PINTXMINUSB	P26	O	Transmit minus B	X2-39
SATA_CLK_IN	V27	I	Clock in	X2-23
RXA	R1	I	Serial receiver, lane A, positive data	X2-11
SATA_CLK_IN# / NC		I	Clock in inverted (complement), if SATA RefClk Compatibility option is present (see 3.2.5.9) No connect otherwise	X2-19
RXA#	P1	I	Serial receiver, lane A, negative data (complement)	X2-15
TXA	P4	O	Serial transmitter, lane A, positive data	X2-22
RXB	U1	I	Serial receiver, lane B, positive data	X2-3
TXA#	N4	O	Serial transmitter, lane A, negative data (complement)	X2-26
RXB#	V1	I	Serial receiver, lane B, negative data (complement)	X2-7
TXB	U4	O	Serial transmitter, lane B, positive data	X2-6
SD_REF_CLK	R5	I	SerDes PLL reference clock	X2-14
TXB#	V4	O	Serial transmitter, lane B, negative data (complement)	X2-10
SD_REF_CLK#	R4	I	SerDes PLL reference clock (complement)	X2-18

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Signal	CPU pin	Type	Description	Module pin
Non-CPU pins (signals not at the CPU, but at the module plug connector)				
RTC_INT#	1	O	Real time clock interrupt outputs INTA# and SQW/INTB# connected together, pull-up 10 kΩ via Schottky diode to VCC3V3	X1-44
TEMP_OS#	1	O	Temperature sensor excess temperature shutdown output	X1-42
RESIN#	1	I	Reset Input (Reset input of voltage supervisor), pull-up 4.7 kΩ	X1-40
CLKOE	1	I	Internal 66.6667 MHz enable, pull-up 4.7 kΩ	X1-45
SEL_CLKIN_DIV	1	I	Select CLK divider, see 3.2.3.1	X1-41
SEL_RESET_SOURCE	1	I	Select reset source. Tri-state input, see 3.2.3.1	X1-43
PLD_TDI	1	I		X1-17
PLD_TDO	1	O		X1-18
Module supply				
VCC3V3ID	4	VCC	3.3 V supply, filtered, directly used for 3.3 V logic	X1-1, X1-2, X1-3, X1-4
VCC3V3IF	6	VCC	3.3 V supply, filtered, DC/DC converter input voltage	X1-5, X1-6, X1-7, X1-8, X1-9, X1-10
LVDD1_OFF	1	VCC	TSEC1 I/O supply voltage, connect to either VCC3V3 or VCC2V5, depending on Physical Interface Mode	X1-23
LVDD2_ON	1	VCC	TSEC2 I/O supply voltage, connect to either VCC3V3 or VCC2V5, depending on Physical Interface Mode	X1-24
VCC3V3	1	VCC	Internal 3.3 V supply after power sequencing switch, use only for LVDD1_OFF / LVDD2_ON supply!	X1-21
VCC2V5	1	VCC	Internal 2.5 V supply, use only for LVDD1_OFF / LVDD2_ON supply!	X1-22
VBAT	1	VCC	Battery Voltage, connected directly to RTC supply pin and ORed VCC3V3 via Schottky diode	X1-46
DGND	X1-36, X1-37, X1-51, X1-52, X1-61, X1-68, X1-73, X1-74, X1-81, X1-82, X1-93, X1-94, X1-106, X1-107, X1-112, X1-117, X1-118, X1-129, X1-130, X1-141, X1-142, X1-153, X1-154, X2-1, X2-4, X2-5, X2-8, X2-9, X2-12, X2-13, X2-16, X2-17, X2-20, X2-21, X2-24, X2-25, X2-28, X2-29, X2-32, X2-33, X2-36, X2-37, X2-40, X2-41, X2-44, X2-49, X2-52, X2-63, X2-64, X2-75, X2-76, X2-87, X2-88, X2-99, X2-100, X2-111, X2-112, X2-123, X2-124, X2-137, X2-138, X2-151, X2-152				
Reserved				
X1_RES1			Reserved for future use	X1-100
X1_RES2			Reserved for future use	X1-102
X1_RES3			Reserved for future use	X1-104
X1_RES4			Reserved for future use	X1-64
X1_RES5			Reserved for future use	X1-65
X1_RES6			Reserved for future use	X1-97
X1_RES7			Reserved for future use	X1-98
Reserved	F1	I/O	Reserved	X1-13
X2_RES1			Reserved for future use	X2-101
X2_RES2			Reserved for future use	X2-102
X2_RES3			Reserved for future use	X2-103

Table 11: Pinout according to function groups

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3.5 Cooling

3.5.1 Power dissipation

Maximum power dissipation of the module (400/267 MHz core/CSB): 5.28 W

3.5.2 Heat sink

Operation without heat sink is possible on the work bench / at room temperature.

In most cases a heat sink PINBLOC 2525-049-04.6 (Schneider Clauss GmbH & Co KG) should be sufficient.

The necessary heat sink depends of the mode of operation (e.g., clock frequency, installation height, airflow), and can therefore not be universally defined.

3.6 Mechanics

3.6.1 General information

- High pin count SMD plug connectors with 0.8 mm pitch
- The combination with different counterparts allows customisation of the stack height to the height of the parts mounted on the base board
- Double-sided SMD assembly

3.6.2 Dimensions

- Board dimensions 70 × 50 mm (Illustration 9)
- Stack height see Table 12

Expansion stage DDR-SDRAM	Stack height without heat sink max. a + b + c	Free stack height under module min. a - d	Stack height in the range of the CPU, max.
All	10.3 mm	2.26 mm	9.76 mm

Table 12: Stack heights

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3.6.3 Side View TQM8315

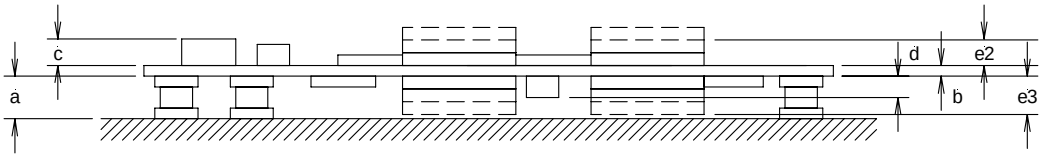

Illustration 8: Stack heights (not to scale)

Dim.	Value [mm]	Remark
a	5.0 ±0.2	Combination module connector with counterpart; with other plug connector on base board 6, 7 and 8 mm are possible
b	2.0 ±0.1	Printed circuit board
c	3.0 +0 / –x	Coil L1 (highest stack height top side)
d	2.54 +0 / –x	Watch crystal (highest stack height bottom side)
f	2.46 +0 / –0.46	CPU (top side, not drawn)

Table 13: Distances

3.6.4 Top View through TQM8315

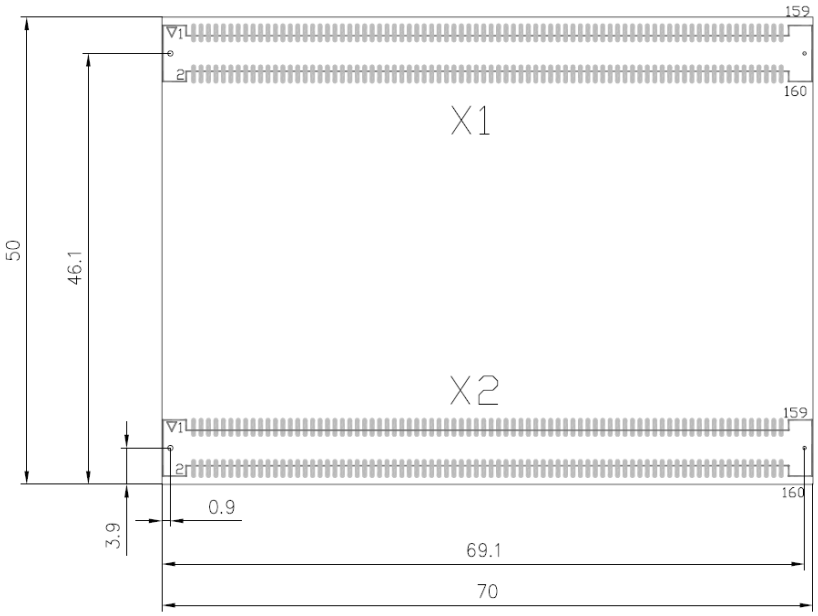

Illustration 9: View from top side through printed circuit board

Note:

2.5 mm should be kept free on the base board, along the longitudinal edges on both sides of the module for the extraction tool MOZI831x.

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3.6.5 Notes of treatment

To avoid damages caused by mechanical stress, it is recommended to extract the TQM8315M from a base board only by using the special extraction tool. It can, however, also be obtained separately.

Please contact your sales representative of TQ-Components.

3.7 Software

The boot loader "U-Boot" is the basic software delivered with the TQM8315M.
For more information see separate specification.

3.8 Safety requirements and protective regulations

3.8.1 EMC

The module was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- With metal casings, a good (at least according to RF) connection to the printed circuit board or to the potential of the housing
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding
- Filtering of all signals which can be connected externally (also "slow" and DC can radiate RF indirectly)

3.8.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the base board, no special preventive measures were planned on the module. According to the data sheets, the used devices already have some protection; however, this is generally not sufficient to fulfil the legal requirements without any further measures.

Following measures are recommended:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, perhaps Zener diode
- Fast signal lines: Integrated protective devices (suppressor diode arrays)

3.8.3 Reliability and service life

The subassembly is designed for a service life of 10 years. It was also designed to be insensitive to vibration and impact.

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3.8.4 Climate conditions and operational conditions

- Protection class IP00

The possible temperature range strongly depends on the installation situation, (heat dissipation by conduction and convection). Hence, no fixed value can be given for the whole assembly. Reliable operation is generally achieved when the following conditions are met:

- Standard temperature range
  - Chip temperature of the CPU: 0 … +105 °C
  - Package temperature of the remaining ICs: 0 … +70 °C
- Extended temperature range
  - Chip temperature of the CPU: –40 … +105 °C
  - Package temperature of the remaining ICs: –40 … +85 °C

Detailed information to the thermal characteristics of the CPU is found in [2]. Information about example configurations with active and passive cooling can be obtained from TQC support.

- Relative air humidity (operation / storing): 10 … 90 % (not condensing)

3.8.5 Environment protection

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

The energy consumption of this subassembly is minimised by suitable measures.

Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (**p**oly**c**hlorinated **bi**phenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

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4. Appendix

4.1 Acronyms and definitions

The following terminology and abbreviations are used:

Acronym	Meaning
BGA	Ball Grid Array
BST	Boundary Scan Test
CAN	Controller Area Network
CE	Communication Engine (= QUICC Engine)
CIB	Configuration Info Block
COP	Common On-Chip Processor
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DDR	Double Data Rate
DMA	Direct Memory Access
DUART	Dual Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic compatibility
eSATA	external Serial ATA
ESD	Electrostatic Discharge
eTSEC	enhanced Three-Speed Ethernet Controller
Flash	Erasable Programmable Read-Only Memory
FR-4	Flame Retardant 4
GMII	Gigabit Media Independent Interface
GPCM	General Purpose Programmable Machines
GPIO	General Purpose Input/Output
I/O	Input/Output
I²C	Inter-Integrated Circuit
ICT	In-Circuit Test
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LSB	Least Significant Bit
MII	Media Independent Interface
MLC	Multi Level Cell
MSB	Most Significant Bit
ODT	On-Die Termination
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect express
PLD	Programmable Logic Device
POST	Power-On Self Test
PQ	Product Qualification
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real-Time Clock
SATA	Serial ATA
SDRAM	Synchronous Dynamic Random Access Memory
SGMII	Serial Gigabit Media Independent Interface
SLC	Single Level Cell
SMD	Surface Mounted Device
SPI	Serial Peripheral Interface
TSEC	Three-Speed Ethernet Controller
TSOP	Thin Small-Outline Package
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
UPM	User Programmable Machines
USB	Universal Serial Bus

Table 14: Acronyms

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4.2 References

[1] MPC8315E PowerQUICC II Pro Integrated Host Processor
Family Reference Manual
MPC8315ERM Rev. 1, Freescale Semiconductor Inc. 2/2008

[2] MPC8315E PowerQUICC™ II Pro Processor
Hardware Specifications
MPC8315EEC Rev. 0, Freescale Semiconductor Inc. 05/2009

[3] Chip Errata for the MPC8315E
MPC8315ECE Rev. 0, Freescale Semiconductor Inc. 02/2009

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